Reduced Capacitor Voltage Stress and Inductor Current of Improved Z-Source Inverter

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Abstract: This paper demonstrates the advantages of an improved Z-Source inverter topology on basis of two major factors that is capacitor voltage stress and inrush current in comparison with the basic topology. The control strategy used is exactly same for both these approaches. Also results obtained are compared with the help of detailed simulation which depicts that the inrush current and capacitor voltage stress has been greatly reduced in the improved scheme. Analysis and simulation results have been compared using MATLAB environment.

Keyword — Inrush current, capacitor voltage stress, simple boost control.

I. INTRODUCTION

There exist two traditional inverters: Voltage Source and Current source inverter. The conventional voltage source [VSI] which is most commonly used inverter type cannot boost the input source voltage. Therefore, it has the following drawbacks: 1) VSI is a buck i.e. step-down inverter for DC-to-AC power conversion and boost i.e. step-up for AC-to-DC power conversion. 2) Upper and lower switches of the same leg cannot be triggered at the same instant. 3) Further power loss is barred by VSI because of use of output LC filter which also increases the control complexities. In addition, both the traditional converters have the following common problems: 1) They are either a step-up (boost) or a step-down (buck) converter and cannot be a buck-boost converter. Thus, their obtainable output voltage range is limited to either greater or smaller than the input voltage. 2) Their major circuits cannot be interchangeable. 3) They are susceptible to EMI noise [1].

To overcome the above problems of the traditional Voltage source and Current source converters, this paper presents an impedance-source power converter (Z-source converter). It is a single-stage inverter topology that demonstrates both buck and boost power conversion capability [1]. In addition, the two switches in the same phase leg can be triggered on at the same time and no dead time is needed, so the output distortion is greatly reduced and the reliability can be improved [12]. It has an additional zero state known as the shoot-through state which was forbidden in the traditional VSI. In spite of the aforesaid merits, the traditional Z-source inverter topology shows the following drawbacks: 1) The capacitor voltage stress is very high which leads to use of higher voltage rating of capacitor; 2) The inrush current cannot be concealed because of which the current and voltage surge occurs that can destroy the device. In case of traditional VSI, capacitor is used for the purpose of storing energy and inductor in case of CSI is used for suppressing current ripple. But the basic topology uses a combination of both these elements for the purpose of storing as well as filtering [2][14].

A new Z-source inverter topology is presented known as the Improved Z-Source Inverter which solves the above stated problems encountered in case of traditional Z-Source inverter that is reduced capacitor voltage stress and inherent inrush current limitation at startup. The operating principle and association with the traditional topology divulge the merits of the proposed topology, and are also established through simulation by MATLAB/Simulink.

II. Z-Source Inverter

The design of traditional 3-phase Z-source inverter is shown in Fig. (1). It comprises of 2 identical inductors and 2 identical capacitors which form a unique impedance network to avoid short circuit when the devices are in shoot through mode. A diode is connected in series with the DC supply to block reverse current. In other words, it consists of an impedance network which is connected just before the conventional 3-phase voltage source inverter. In 3-phase Z-source inverter, an additional control parameter is introduced, namely the Boost Factor (B), which modifies the AC output voltage equation of conventional 3-phase voltage inverter as:
where, \( v_{\text{out}} \) is maximum sinusoidal inverter output voltage, \( B \) is the boost factor, \( M \) is the modulation index and \( V_0 \) is the DC Input voltage.

Fig. 1 Z-Source Inverter Topology

A. Z-capacitor Voltage Stress:

As described in [1], the crest dc link voltage can be expressed as:

\[
V_i = \frac{B V_o}{1 - 2D_o} \tag{2}
\]

where, \( V_o \) is DC input voltage and \( B \) is the Boost Factor. The boost factor, \( B \) can be varied by varying the duty cycle, \( D_0 \). The capacitor voltage is given by:

\[
V_c = \frac{V_o}{2D_o} \tag{3}
\]

As seen from equation (2), \( V_c \) isn’t less than \( V_o \), thus the capacitor voltage stress is on the higher side for the traditional Z-source inverter.

B. Inrush Current at Startup:

In case of Z-Source Inverter, a huge inrush current exists at startup as shown in fig. (2). The initial voltage across the capacitors is zero, so the huge inrush current charges the Z-capacitors immediately to 0.5\( V_o \) and this leads to resonance problem. The ultimate result is large Z-capacitor voltage surge and Z-inductor current surge.

Fig. 2 High Inrush current

Fig. 3 Improved Z-Source Topology

III. IMPROVED Z-SOURCE INVERTER

Fig (3) represents the Improved Z-Source Inverter topology. The elements used are exactly similar to that used in case of traditional Z-Source inverter. The difference is in the arrangement in which the impedance network and the inverter bridge are placed. In the improved topology, the position of the Inverter Bridge and diode is exchanged and their connection direction is inverted. The voltage polarity of the capacitors in the proposed topology has the same input voltage polarity; therefore, the capacitor voltage stress can be greatly abridged and the same boost voltage across the inverter bridge can be procured. The topology has inherent constraint to inrush current as compared to the previous topology since there is no current path at startup.

IV. OPERATING PRINCIPLE AND COMPARATIVE EVALUATION OF BOTH TOPOLOGIES

The equivalent circuit diagram of improved Z-Source inverter is shown in fig (4). Since the inductors and capacitors used in the impedance network are identical:

\[
V_{C1} \quad V_{C2} \quad V_C
\]

\[
V_{L1} \quad V_{L2} \quad V_L
\]

Fig. 4. Equivalent circuit of Z-source inverter when Inverter Bridge is operating in traditional active mode
Fig. 5. Equivalent circuit of Z-source inverter when Inverter Bridge is operating in traditional zero state

During shoot through state, the inverter is shorted as shown in fig (6), we get

\[ v_L = v_O = v_C \]  \hspace{1cm} (5)

When in non-shoot through state i.e. active and null state, inverter side can be simplified as a current source as shown in fig (4). The following equation can be derived for this state;

\[ v_L = v_C \]  \hspace{1cm} (6)

Therefore, we get the following equation;

\[ v_C = \frac{D_O}{12D_O} v_O \]  \hspace{1cm} (7)

It is evident from the eq. (7) that when the shoot-through duty ratio, \( D_O \) is zero, then the Z-Source capacitor voltage is also zero. The peak dc-link voltage across the inverter and peak output phase voltage can be expressed as;

\[ V_P = \frac{1}{B} \left( V_m E_s \right) \]  \hspace{1cm} (8)

where \( B \) is the boost factor determined by \( D_O \) and \( M \) is the modulation ratio. The output voltage is boosted by a factor \( B \) (\( B \geq 1 \)), which is the same as the previous topology.

A. Z-Source Capacitor Voltage Stress and Voltage Ripple:

By comparing eq. (7) and eq. (8), we can see that the dc-link voltage for both the approaches is exactly same. Therefore, the boosted voltage remains the same for both the topologies. The Z-Source capacitor voltage decreases with decrease in \( V_O \) as seen in eq. (7) for the improved topology when compared with the basic configuration which is evident in eq. (3). The condition for previous and improved Z-source inverter is exactly same during shoot-through period.

B. Z-Source Inductor Current:

The average Z-source inductor current in both the approaches are same. During shoot-through state, the Z-source inductor current decreases for improved topology and the current ripple is given by;

\[ i_L = \frac{(1 - D_O) TV_o}{L} \]  \hspace{1cm} (10)

As compared to eq. (10), the current ripple for the previous configuration increases during the shoot-through state and can be expressed as;

\[ i_L = \frac{D_O TV_o}{L} \]  \hspace{1cm} (11)

V. CONTROL STRATEGY FOR TOPOLOGIES

The control strategy used in this paper is Simple Boost Control. In this control strategy, two straight lines are used as upper and lower shoot-through reference lines. Whenever the triangular waveform is greater than the straight line all the upper switching devices are switched ON whereas the lower devices are already ON causing shoot-through and vice-versa. The ST duty ratio decreases with increase in Modulation Index as depicted by the simulation results as shown in fig (4)

For Simple Boost Control technique, the practical values of capacitor and inductor required in the impedance network can be calculated using the expression given below. For finding value of capacitor, \( C \);

\[ C = \frac{3T_s I_m \cos \left( \frac{2V_m E_s}{4V_m E_s} \right)}{8k v E_s} \]  \hspace{1cm} (12)
For finding value of inductor, $L$:

$$2T, E, (2V_{m} - E_{r})$$

$$L = \frac{3kI_{m} \cos (4V_{m} - E_{r})}{(13)}$$

**SIMULATION RESULTS**

Simulation results are given to demonstrate the advantages of Improved Z-source inverter compared to the basic topology by two factors i.e. capacitor voltage stress and inductor current. The control strategy used is simple boost control which is same for both the topology. The same results can be verified using other control strategies like maximum boost control and constant-boost control. The parameters selected for simulation are:

- Input voltage $V_{o}=150$V;
- Load: three-phase R-L load, $R=10\Omega$, $L=0.032$H;
- Z-Source Network: $L_{1}=L_{2}=190$mH, $C_{1}=C_{2}=1000\mu$F;
- Switching frequency: 10kHz

![Simulation results under D=0.3, M=0.7 of traditional topology](image)

**Fig. 8. Simulation results under D=0.3, M=0.7 of traditional topology**

**Fig. (8) and (9) show the simulation results of conventional and improved topologies respectively when Do= and M=0.7.** The waveform from top to bottom are line voltage $V_{line}$, phase voltage $V_{ph}$, capacitor voltage $V_{C}$, inductor current $I_{ind}$, input voltage $V_{in}$ and inverter input voltage $V_{inv}$ respectively. In the basic topology, we can see that the capacitor voltage is exactly same as the inverter input voltage.

Moreover huge amount of inrush current occurs at startup which makes the inductor current to be large. Thus, the conventional topology has large capacitor voltage stress and large inductor current which leads to setting of resonance condition that ultimately leads to voltage and current surges. Therefore, the converter can be destroyed completely and for the model to work successfully, a higher rating of the inductor and capacitor is required.

In case of improved topology, the capacitor voltage is not equal to the inverter input voltage. The simulation results clearly depict the fact that in both these topologies the boosted inverter voltage remains the same. Therefore, the boost factor remains the same but the drawbacks occurring in the traditional model is overcome by using this topology.

![Simulation results under D=0.3, M=0.7 of improved topology](image)

**Fig. 9. Simulation results under D=0.3, M=0.7 of improved topology.**

**Figs.(10)-(11) shows the simulation results for D=0.25 and M=0.75.** We can see that the capacitor voltage is greater than the inverter voltage and inrush current is on the higher side. This improved topology on the other hand has reduced capacitor voltage as well as inrush current. Figs 12-13 depicts the simulation results with D=0.2 and M=0.8. It is evident from the simulation results that the advantages proposed by the improved topology are far better as compared to the traditional topology.
Fig. 10. Simulation results under D=0.25, M=0.75 of traditional topology

Fig. 11. Simulation results under D=0.25, M=0.75 of improved topology

Fig. 12. Simulation results under D=0.2, M=0.8 of traditional topology

Fig. 13. Simulation results under D=0.2, M=0.8 of improved topology
TABLE I. TOPOLOGY COMPARISON WITH RESPECT TO \textit{I}_{\text{mp}} \text{ AND} V_C

<table>
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<th>Inv. Topology</th>
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<tr>
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<td>\textit{M}</td>
<td>\textit{B}</td>
<td>\textit{V}_{\text{IN}} [V]</td>
<td>\textit{V}_{\text{CC}} [V]</td>
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VII. CONCLUSION

This paper has demonstrated the advantages of Z-source inverter topology. Compared to the traditional one, the improved topology has several virtues:

1) The Z-capacitor voltage stress is reduced by inverter input voltage to perform the same boost capacity. Thus, a lower voltage rating of Z-capacitor can be utilized to reduce the system cost and volume.

2) The in-rush current at start up is reduced in the proposed topology.

REFERENCES
