International Journal of Engineering Research in Electronics and Communication Engineering (IJERECE) Vol 1, Issue 1, Dec 2014

Implementation of High Precision Fixed Width Multiplier for DSP Applications

[1] G.Niharika,[2] B.Santosh Kumar
[1] PG Scholar, Department of Electronics & Communication, Vaagdevi College of Engineering Warangal India-506005
[2] Assistant Professor, Department of Electronics & Communication, Vaagdevi College of Engineering Warangal India-506005
[1] niharika_rec@hotmail.com, [2]Santosh_b34@yahoo.com

Abstract: **Significant improvements in area, delay, and power can be achieved with truncated multipliers. Fixed-width multipliers generate n-bit (instead of 2n-bit) products with low product error, but use only about half the area and less delay when compared with a standard parallel multiplier. In them, cost-effective carry-generating circuits are designed, respectively, to make the products generated more accurately and quicklyThe proposed method aims at tree reduction using proper ratio of full adders and half adders. The advantage of doing so, is experimentally we can achieve better area. The output is in the form of LSB and MSB. Using the most significant methods like reduction, deletion, truncation, rounding and final addition in order to compress the LSB part. In previous related papers, to reduce the truncation error we use error compensation circuits. But here, there is no need of error compensation circuits, and the final output is precise.**

Keywords: **Computer arithmetic, faithful rounding, fixed- width multiplier, tree reduction, and truncated multiplier.**

I. INTRODUCTION

MULTIPLICATION is one of the most area consuming arithmetic operations in high-performance circuits. As a consequence many research works deal with low power design of high speed multipliers. Multiplication involves two basic operations, the generation of the partial products and their sum, performed using two kinds of multiplication algorithms, serial and parallel.

Serial multiplication algorithms use sequential circuits with feedbacks: inner products are sequentially produced and computed. Parallel multiplication algorithms often use combinational circuits and do not contain feedback structures. Multiplication of two bits produces an output which is twice that of the original bit. It is usually needed to truncate thepartial product bits to the requiredprecision to reduce area cost. Fixed-width

Multipliers, a subset of truncated multipliers, compute only n most significant bits (MSBs) of the 2n bit product for n×n multiplication and use extra correctio n/compensation circuits to reduce truncation errors.

In previous related papers, to reduce the truncation error by adding error compensation circuits. So that the output will be précised.

In this approach jointly considers the tree reduction, truncation, and rounding of the PP bits during the design of fast parallel truncated multipliers so that the final truncated product satisfies the precision requirement.

In our approach truncation error is not more than 1ulp (unit of least position), so there is no need of error compensation circuits, and the final output will be précised.

II. REDUCTION SCHEMES OF PARALLEL MULTIPLIERS

PP (partial product) generation produces partial product bits from the multiplicand and multiplier. PP reduction is used to compress the partial product bits to two. Finally the partial products bits are summed by using carry propagate addition. Two famous reduction methods are available,

1. Dadda tree
2. Wallace tree

Dadda reduction performs the compression operation whenever it required. Wallace tree reduction always compresses the partial product bits. In the proposed method,

uses RA reduction method. So that the final bit will be reduced.

In the proposed truncated multiplier design, introduces column-by-column reduction. Here two reduction schemes are used, to minimize

the half adders in each column because the full adder has high compression rate when compared to HA.

A. Scheme1 and Scheme2

Fig. 1 shows the reduction procedure of Scheme 1, reduction starting from the least significant column. Column height is h, including the carry bits from least significant columns, are also shown on the top row where the columns that need HAs are highlighted by square boxes. Fig. 2 shows the technology schematic of scheme 1 using Mentor Graphics.

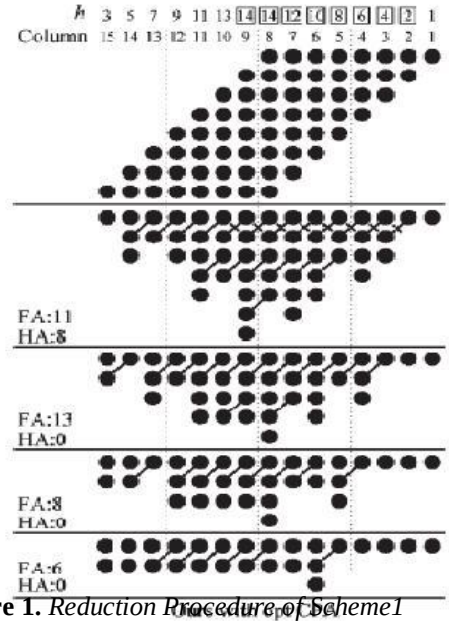

Figure 1. *Reduction Procedure of Scheme1*

These methods mainly discuss about the cost compensation. By comparing the methods of Dadda, Wallace and RA with scheme1 and Scheme2, the reduction of bits are better, so the area can be saved higher than the former methods. From the literature survey it is clear that various researchers are working in these areas to optimize the same. Compression ratio also takes up its major concern here, were it plays a crucial role when output precision is concerned. Fig. 3 shows the reduction procedures by scheme 2 to each column of partial product bits, reduction starting from the least significant column.

Scheme 1 having minimum CPA (carry propagate addition) bit width as twice reduction efficiency when compared to the Wallace method which produces the same result as that of RA method.

Fig. 2 Shows reduction procedure of scheme2. Scheme 1 is only used to determine whether an HA is needed and how many FAs are required in the per-column reduction that does not exceed the maximum number of Carry Save Additions in reduction levels.

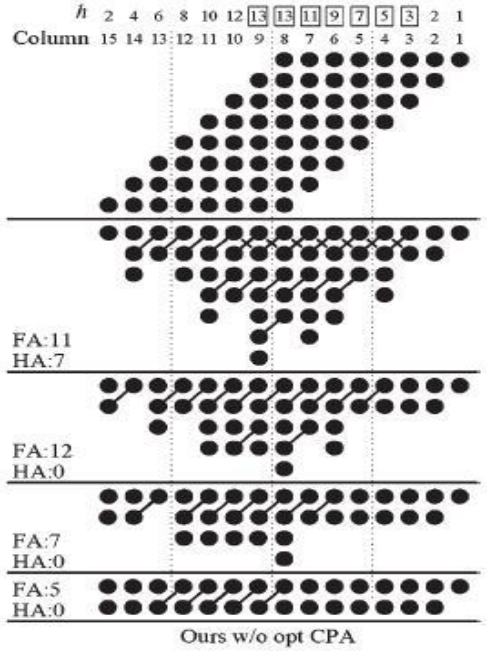

Figure 2.*Reduction Procedure of Scheme2*

The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 13.2. From the synthesized results, the scheme 1 and scheme 2 has 1056 and 822 number of gates. The proposed multiplier has only 582 gates.Area utilization by the proposed method is less when compared to scheme 1 and scheme 2.

III. PROPOSED TRUNCATED MULTIPLIER

The objective of a good multiplier is to provide a physically compact, good speed and low power consuming chip. To save significant power consumption of a VLSI design. In a truncated multiplier, several of the least significant columns of bits in the partial product matrix are not formed. Figure 5 Show 8x8 truncated multiplication.(a) deletion, reduction and truncation. (b) Deletion, reduction, truncation, and final addition.

In the first step deletion operation is performed, that removes all the avoidable partial product bits which are shown by the light gray dots (fig 3). In this deletion operation, delete as many partial product bits as possible. Deletion error E_D should be in the range $-1/2$ ulp $\leq E_D \leq 0$.Hereafter, the injection correction bias constant of 1/4 ulp.

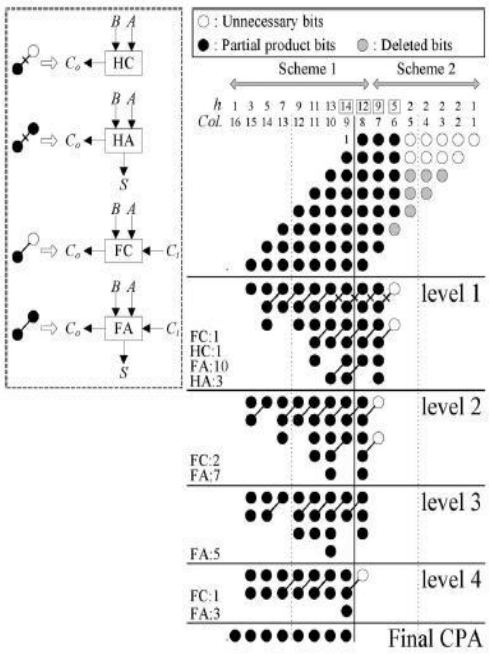

Figure 3.*Proposed Truncated Multiplier*

The deletion error after the bias adjustment $-1/4$ ulp $\leq E_D \leq 1/4$ ulp. In Fig. 5, the deletion of partial product bitsstarts from column 3 by skipping the first two of partial product bits. After the deletion of partial product bits, perform column-by-column reduction of scheme 2. After the reduction, perform the truncation, which will further remove the first row of (n -1) bits from column 1 to column (n-1). It will produce the truncation error which is in the range of $-1/2$ ulp $\leq E_T \leq 0$. Hence introduction of another bias constant of ¼ ulp in truncation part. So the adjusted truncation error is $-1/4$ ulp $\leq E_T \leq 1/4$ ulp.

B. Rounding and Final Addition

All the operations (deletion, reduction, and truncation) are done, finally the PP bits are added by using CPA (carry propagate addition) to generate final product of P bits. Before the final CPA, add a bias constant of ½ ulp for rounding. Rounding error is in the form of $-1/2$ ulp $\leq E_R \leq 1/2$ ulp. The faithfully truncated multiplier has the total error in the form of $-\text{ulp} < E = (E_D + E_T + E_R) \leq \text{ulp}$.

C. Proposed Algorithm

In proposed architecture we can multiply 8x8 bits, and the bits are reduced in step by step manner. Deletion is the first operation performed in Stage 1 to remove the PP bits, as long as the magnitude of the total deletion error is no more than 2^{-P-1}.Then number of stages to reduce the final bit width without increasing the error.

In normal truncated multiplier design, the architecture produces the output with some truncation error. But in the proposed design of truncated multiplier the truncation error is not more than 1 ulp, so the precision of the final result is improved. Fig. 3 shows proposed truncated multiplier. This reduces the area and power consumption of the multiplier. It also reduces the delay of the multiplier in many cases, because the carry propagate adder producing the product can be shorter.

IV. IMPLIMENTATION OF FUTURE ENHANCEMENT

Truncated multiplier can be effectively implemented in FIR filter structure. Conventional FIR filer performs ordinary multiplication of co-efficient and input without considers the length.

Thus the structure can be made effective by replacing the existing multiplier with the proposed fixed width truncated multiplier for visible area reduction. Fig. 4 shows the architecture of FIR Filter.

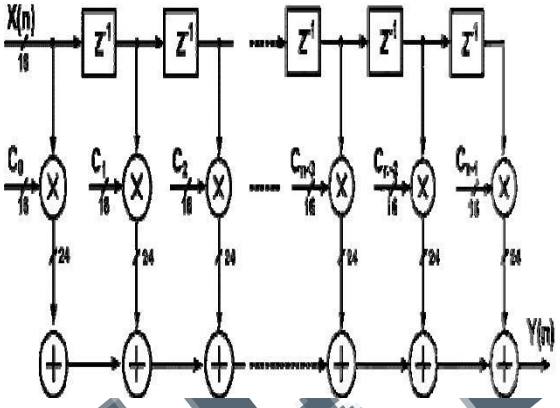

Figure 4.*Fir Filter*

V. EXPERIMENTAL RESULTS

By using the Synthesis tool is Modelsim..The proposed system is implement-ed by using FPGA-Spartan 3E.This methods are mainly applicable in DSP systems.

A. Power Analysis

The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 13.2. From the synthesized results, it is found that the scheme 1 consumes 185mW, scheme 2 consumes 176mW. The proposed multiplier consumes low power of 88mW when compared to scheme 1 and scheme 2.

B. Area Analysis

Table 1.*Area Analysis of the Scheme 1, 2 & Proposed*

Parameter	Scheme 1	Scheme 2	Proposed
No. of Gate counts	1056	822	582

The table 1 shows that the proposed method reduces the power and area than the previous methods. When compared to previous methods the precision is improved.

VI. SIMULATION RESULTS

Figure 5. *Scheme1 Results*

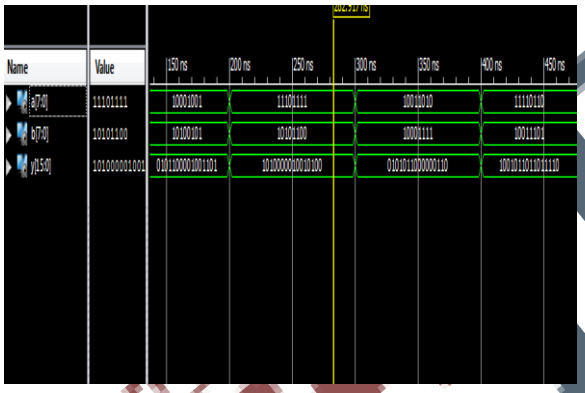

Figure 6. *Scheme2 Results*

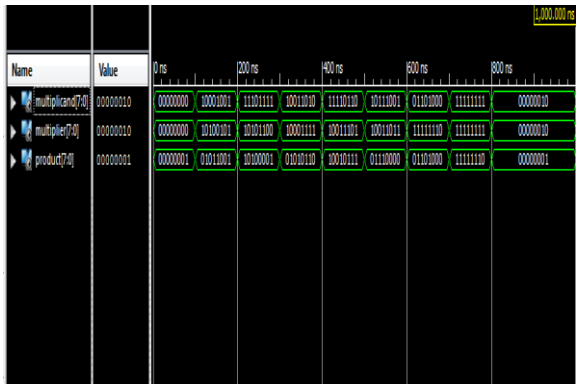

Figure 7.*Proposed Fixed Width Multiplier*

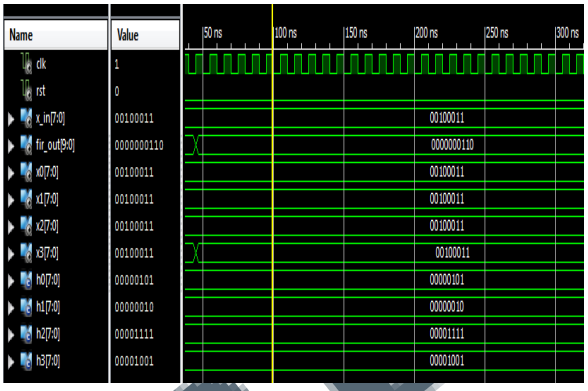

Figure 8.*Fir with Proposed Multiplier*

CONCLUSION

There are many works proposed to reduce the truncation error by adding error compensation circuits so as to produce a précised output. In this approach jointly considers the tree reduction, truncation, and rounding of the PP bits during the design of fast parallel truncated multipliers, so that the final truncated product satisfies the precision requirement.
In this approach truncation error is not more than 1ulp, so there is no need of error compensation circuits, and the final output will be précised. The scheme1, scheme2 and proposed multiplier architecture has been simulated and synthesized using XILINX ISE Design Suite 8.1.
From the synthesized results, it is found that the scheme 1 consumes 185mW, scheme 2 consumes 176mW. The proposed multiplier consumes low power of 88mW when compared to
scheme 1 and scheme 2. The scheme 1and scheme 2 has 1056 and 822 number of gates. The proposed multiplier has only 582 gates. Area utilization by the proposed method is less when compared to scheme 1 and scheme 2.

REFERENCES

[1] J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of low-error fixed- width multipliers for DSP applications," IEEE Trans. Circuits Syst. II, s Analog Digit. Signal Process., vol. 46, no. 6, pp. 836–842, Jun. 1999.

[2] L.-D. Van and C.-C. Yang, "Generalized low-error area-efficient fixed width multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 8, pp. 1608–1619,Aug. 2005.

[3] M. J. Schulte and E. E. Swartzlander, Jr., "Truncated multiplication with correction constant," in VLSI Signal Processing VI. Piscataway, NJ:IEEE Press, 1993, pp. 388–396.

[4] E. J. King and E. E. Swartzlander, Jr., "Data-dependent truncation scheme for parallel multipliers," in Proc. 31st Asilomar Conf. Signals, Syst. Comput., 1997, pp. 1178– 1182.

[5] M. J. Schulte, J. G. Hansen, and J. E. Stine, "Reduced power dissipation through truncated multiplication," in Proc. IEEE Alessandro Volta Memorial Int. Workshop Low Power Des., 1999, pp. 61–69.

[6] T.-B. Juang and S.-F. Hsiao, "Low-error carry-free fixed-width multipliers with low-cost compensation circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 6, pp. 299–303, Jun. 2005.

[7] A.G.M. Strollo, N. Petra, and D. De Caro, "Dual-tree error compensation for high-performance fixed-width multipliers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol.52, no. 8, pp. 501–507, Aug. 2005.

[8] E. G. Walters and M. J. Schulte, "Efficient function approximation using truncated multipliers and squarers," in Proc. 17th IEEE Symp. ARITH, 2005, pp. 232–239.

[9] C. S. Wallace, "A suggestion for a fast multiplier," IEEE Trans. Electron. Comput., vol. EC-13, no. 1, pp. 14–17, Feb. 1964.